REMARKS

At the time of the Office Action dated December 3, 2002, claims 1-12 were pending. Claims 2 and 9 have been amended to improve wording but their claim scope is not narrowed for any reason relating to patentability. The specification has also been amended to obviate informalities pointed out by the Examiner. Care has been exercised to avoid the introduction of new matter.

Specification Objections

The disclosure has been objected to because of informalities. In response, the informality on page 1, line 16 of the disclosure has been addressed in a manner consistent with the Examiner's suggestions. With respect to another informality identified by the Examiner on page 3, lines 18-20 of the disclosure, Applicants have amended it to clarify the language.

Therefore, Applicants solicit withdrawal of the specification objections.

Claim Objections

Claims 2 and 9 have been objected to because they recited the language "in each segment" before a segment is defined. In response, Applicants have amended claims 2 and 9 in a manner consistent with the Examiner's suggestions thereby overcoming the stated bases for the objection to the claims.

Applicants, therefore, solicit withdrawal of the claim objections.

Claims 1-6 and 8-12 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Nagata et al. in view of Shimazaki et al.

In the statement of the rejection, the Examiner admitted that Nagata et al. does not specifically disclose determining the waveform of the source current in the digital circuit from the analysis model. The Examiner then cited Shimazaki et al., concluding that it would have been obvious to one having ordinary skill in the art to modify the invention of Nagata et al. to include determining the waveform of the source current in the digital circuit from the analysis model, as taught by Shimazaki et al. The reasoning is that the combination would have provided a means for conveniently determining the EMI noise characteristics from the current waveform in a time-reducing method. This rejection is traversed.

All the limitations are not taught or suggested by Nagata et al. and Shimazaki et al., either individually or in combination.

In response, Applicants submit that the Examiner has not established *a prima facie* basis to deny patentability to the claimed invention under 35 U.S.C. §103 for lack of the requisite factual basis with respect to independent claims 1, 6 and 8. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Nagata et al. and Shimazaki et al., either individually or in combination, would not have taught or suggested each and every limitation of claims 1, 6 and 8.

It is also submitted that the Examiner must point to "page and line" of a reference wherein each feature of a claimed invention is asserted to reside in denying patentability to a claimed invention based upon prior art. *In re Rijckaert,* 9 F.3d 1531, 28 USPQ2d

1955 (Fed. Cir. 1993). Indeed, as recently held by the Board of Patent Appeals and Interferences, the Examiner must not only point to "column and line of each relevant prior art reference," but must also explain how one having ordinary skill in the art would have interpreted each of the relied upon portions of the cited references. *Ex parte Gambogi,* 62 USPQ2d 2019 (BPAI 2001). That burden has not been discharged.

First, Applicants emphasize that Nagata et al. does not disclose the claimed invention for the following reasons.

As a time elapses, operation of a logic circuit changes and a noise waveform changes. For this reason, the claimed invention provides a simulation model for analyzing a temporal variation of a source current waveform, which expressly represents the transfer of electric charge due to continuous operations of logic circuits by connecting parasitic capacitors to a source or ground line to charge them in time series (in chronological order).

On the other hand, Fig. 7 of Nagata et al. shows a physical model which indicates that a high speed switching operation of a logic circuit can be achieved by a transfer of electric charge between parasitic capacitors. Fig. 7 merely represents logic operation and noise generated at a certain instant or moment.

Specifically, it is apparent that Nagata et al. does **not disclose a parasitic capacitor series including parasitic capacitors to be charged in time series,** recited in claims 1, 6 and 8, and the Examiner did **not point out** where in Nagata et al. those capacitors are disclosed. What Nagata et al. discloses are parasitic capacitors to be charged or discharged and parasitic capacitors in a stable charged state at a certain instant. It is noted that the Examiner's cited portions, page 577, column 1, paragraph 5

and Figure 7, are silent on the above limitation recited in the claims. The Examiner's burden has not been discharged. *In re Rijckaert*; *Ex parte Gambogi, supra*.

Applicants further submit that Nagata et al. is silent on an analysis of the source current. For example, the Examiner cited the paragraphs of Nagata et al. and asserted that "Nagata also discloses that the source current from the analysis model along with the parasitic impedances of the source and ground lines causes a voltage variation, regarded as substrate noise" (the ultimate sentence at page 3 of the Office Action). Despite the Examiner's assertion, it is apparent that the Examiner's cited portions as well as other portions of Nagata et al. do not disclose the analysis of the source current. Again, the Examiner's burden has not been discharged. *In re Rijckaert*; *Ex parte Gambogi, supra*.

Accordingly, Nagata et al. does not disclose and the Examiner did not point to all the limitations recited in claims 1, 6 and 8.

Second, Applicants submit that Shimazaki et al. does not disclose the claimed invention. Shimazaki et al. discloses obtaining a source current waveform in an LSI including a plurality of logic gates by approximating a source current generated in a switching operation for each logic gate by a triangular current waveform and merging each triangular current in a whole circuit.

On the contrary, the claimed invention, based on that a high speed switching operation of a logic circuit can be achieved by the transfer of electric charge between parasitic capacitors, obtains a source current waveform in LSI by generating, in time series or in chronological order, a charging step of parasitic capacitors for a time interval. The claimed invention and Shimazaki et al. are quite different from each other in basic concepts for the current analysis.

In addition, Shimazaki et al. also does **not** disclose, among other things, a parasitic capacitor series including parasitic capacitors to be charged in time series.

Thus, consideration of the teachings of Nagata et al. and Shimazaki et al., either individually or in combination, would not have suggested each and every limitation of claims 1, 6 and 8. In the instant case, the pending rejection has not established *prima facie* obviousness of the claimed invention as recited in claims 1, 6 and 8, because the proposed combination fails to satisfy the all the claim limitations as required under §103. More specifically, because both references do **not** disclose, among other things, **a parasitic capacitor series including parasitic capacitors to be charged in time series and an analysis model including the parasitic capacitor series**, recited in the claims, the combination of the references never arrive at the claimed invention even if the combination were proper. Applicant, therefore, solicits withdrawal of the rejection of claims 1, 6 and 8.

There is no motivation for modification of Nagata

Applicants also submit that there is no motivation to modify the teaching of Nagata et al. based on that of Shimazaki et al. to arrive at the claimed invention.

In imposing a rejection under 35 U.S.C. §103, the Examiner is required to make a "thorough and searching" factual inquiry and, based upon such a factual inquiry, explain **why** one having ordinary skill in the art would have been realistically impelled to modify particular prior art, in this case the teaching of Nagata et al., to arrive at the claimed invention. *In re Lee,* 277 F.3d 1338, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002). Merely identifying features of a claimed invention in disparate prior art references does not, automatically, establish the requisite motivation for combining references in any

particular manner. *In re Dembiczak,* 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999); *Grain Processing Corp. v. American-Maize Products Co.,* 840 F.2d 902, 5 USPQ2d 1788 (Fed. Cir. 1988). In applying the above legal tenets, it is apparent that the Examiner has **not** established the requisite motivational element.

First, the Examiner asserted "the combination would have provided a means for conveniently determining the EMI noise characteristics from the current waveform in a time-reducing method (2.6 and 2.7)" (emphasis added) (page 5, lines 7-9 in the Office Action). It is submitted that Nagata et al. is silent as to "determining the EMI noise characteristics" and as to the "time-reducing" aspects. This is so because Nagata et al. describes that its purpose is "for experimental studies on substrate noise properties in a mixed signal IC environment" (emphasis added) (page 575, left column, lines 3-4). An equivalent circuit shown in Fig. 7 of Nagata et al. is also used for studying substrate noise properties (see page 575, left column, lines 9-13; page 578, right column, lines 5-8).

Second, one aspect of the claimed invention is to analyze "the waveform of a source current at an enhanced accuracy and higher speed with consideration of re-distribution of charges throughout the digital circuit" (page 4, lines 20-23). Neither Nagata et al. nor Shimazaki et al **disclose** this aspect. Applicants submit that without this aspect, one skilled in the art would not have been motivated to modify the prior art. Nagata et al. and Shimazaki et al. are totally irrelevant to this aspect of the claimed invention because, again, Nagata et al. relates only to experimental studies on substrate noise properties and Shimazaki et al. relates only to EMI noise analysis with gate level simulator.

Third, the Examiner asserted that "Applicant admits as well known in the art... that 'the principal cause of substrate noise generation is a change in voltage generated when the source current of the digital circuits flowing through internal power-supply and ground wirings, ... the generation of noises largely depends on a change in the source current'" (page 5, lines 10-19 of the Office Action). Applicants submit that this assertion is irrelevant to modification of the teaching of Nagata et al. based on that of Shimazaki et al. This is so because the Examiner does not specifically show how his assertion would have given one skilled in the art motivation to modify the teaching Nagata et al. based on that of Shimazaki et al. Moreover, Nagata et al. and Shimazaki et al. do not suggest motivation based on the facts asserted by the Examiner.

It should, therefore, be apparent that a *prima facie* basis to deny patentability to the claimed invention has **not** been established for lack of the requisite factual basis and warranted the requisite realistic motivation.

Applicants, therefore, solicit withdrawal of the rejection of claims 1, 6 and 8.

Dependent claims 2-5 and 9-12.

Dependent claims 2-5 and 9-12 would not have been obvious. If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Accordingly, as claim 1 and 8 are patentable for the reasons set forth above, it is submitted that dependent claims 2-5 and 9-12 which respectively depend on claims 1 and 8 are also patentable. The Examiner's additional comments with respect to claims 2-5 and 9-12 do not cure the argued fundamental deficiencies of Nagata et al. and Shimazaki et al.

Nagata et al. does not disclose a segment defined in claim 2. Regarding claim 2, in order to improve analyzing accuracy for a source current waveform or a noise waveform, an LSI is divided into a plurality of segments based on impedance distribution on source and ground lines in the LSI and then an analysis model is generated for each segment (page 17, line 14 to page 19, line 11 of the specification). Nagata et al. does not disclose such a concept as to the segment.

Applicants traverse the rejections of those claims and solicit withdrawal thereof.

Claim 7 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Nagata et al. in view of Shimazaki et al. and further in view of Mitra et al.

The Examiner asserted that Nagata et al. and Shimazaki et al. do not specifically disclose the limitations "receiving the design specification," "designing the analog and digital circuits...," and "re-designing the analog and digital circuit... by reviewing the result of the substrate noise analysis... ." For this reason, the Examiner cited Mitra et al., asserting that it teaches or suggests those limitations. The Examiner, then, concluded that it would have been obvious to one having ordinary skill in the art to modify the invention of Nagata et al. and Shimazaki et al. based on the teaching of Mitra to include a method for designing the semiconductor integrated circuit including the limitations recited in claim 7. This rejection is traversed.

Claim 7 includes all the limitations recited in claim 6. For the reason set forth above, claim 7 is not obvious because all the limitations recited in claim 6 are not taught or suggested in Nagata et al. and Shimazaki et al. In addition, there is no motivation to

modify the teaching of Nagata et al. based on that of Shimazaki et al to obtain the invention claimed in claim 6.

It should, therefore, be apparent that a *prima facie* basis to deny patentability to the claimed invention has **not** been established for lack of the requisite factual basis and warranted the requisite realistic motivation. Applicants therefore solicit withdrawal thereof.

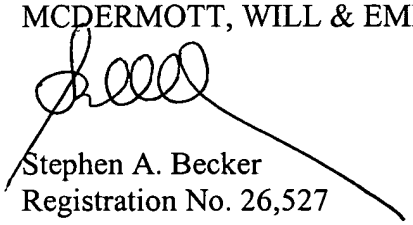
Conclusion.

The imposed rejections have been overcome and all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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APPENDIX

IN THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 13 as follows:

As electronic devices in a large-scale integrated circuit (referred to as "LSI", hereinafter) have been reduced in the size, digital circuits patterned in the LSI are scaled out and improved in [a] an operation speed. However, such LSIs and their application systems generally suffer from degradation in the performance due to the generation of noises which results from a change in the source current flowing across the LSI circuits during the operation.

Please amend the paragraph beginning at page 3, line 7 as follows:

A couple of conventional methods of analyzing the waveform of a source current are referenced. A first method includes expanding the digital circuits to a transistor level and using a circuit simulator for transition analysis thus to examine the waveform of the source current. A second method includes approximating the waveform of a consumed current at each logic gate in the digital circuits to a triangle wave. The triangle wave represents that the charging and discharging processes of load impedance in the switching operation of the logic gate complete within switching time. Then, [and then summing] the waveforms of the currents of the digital circuits are summed to have a waveform of the source current (K. Shimazaki, H. Tsujikawa, S. Kojima, and S. Hirano, "LEMINGS: LSI's EMI-Noise Analysis with Gate Level Simulator", the proceedings of IEEE, ISQED2000). [In the second method, the charging and discharging processes involved in the switching operation complete for a comparable period of switching time.]

IN THE CLAIMS:

2. (Amended) The method according to claim 1, wherein where the digital circuit is divided into a plurality of segments along the border at which the parasitic impedances of the source line and the ground line are locally increased, the parasitic capacitor series and the group of the parasitic capacitors statically charged are assigned for a group of the logic gates included in each segment[, where the digital circuit is divided into a plurality of segments along the border at which the parasitic impedances of the source line and the ground line are locally increased].

9. (Amended) The apparatus according to claim 8, wherein where the digital circuit is divided into a plurality of segments along the border at which the parasitic impedances of the source line and the ground line are locally increased, the parasitic capacitor series and the group of the parasitic capacitors statically charged are assigned for a group of the logic gates included in each segment[, where the digital circuit is divided into a plurality of segments along the border at which the parasitic impedances of the source line and the ground line are locally increased].